REMARKS

Claim 7 stands rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Toyonaga *et al.* (U.S. Patent No. 5,896,055). Applicant traverses the § 102(b) rejection of claim 7 for at least the reasons discussed below.

Toyonaga *et al.* fails to teach or suggest a stage that generates of control signals based on the transition timing of one clock of the plurality of clocks and on phase differences between the plurality of clocks, as recited in claim 7. It is fairly clear from Figures 2 and 3 of Toyonaga *et al.* that the two clocks input at IN1 and IN2 have no relationship to each other such that the control signals received at the alleged switches (diodes, 32, 34) are based on the transition timing of one clock (for example, IN1) or on the phase differences between the two clock signals IN1 and IN2. The clock signals of Toyonaga *et al.* are independent from one another, and are simply buffered by the input buffers (31, 33). There is no teaching or suggestion that signals output from the buffers (31, 32) are based upon phase differences between the input clock signals, or on the transition timing of one of the clock signals.

Toyonaga *et al.* fails to teach or suggest at least a switch group that controls the charging and discharging of a capacitor where clock phase differences vary the charging or discharging speed of the capacitor by shifting the switch control timings of switches in the switch group, as recited in claim 7. First, as implicitly admitted by the Examiner, the NMOS transistor (37) that is connected to the output of the buffer (35) is not part of the switch group, since it is not controlled by the alleged switches (diodes 32, 34) comprising the switch group. Second, in the

circuit shown in Figure 2 of Toyonaga *et al.*, one of ordinary skill in the art would not consider the diodes (32, 34) to be switches that control the charging or discharging of a capacitor. As stated in the disclosure of Toyonaga *et al.*, the diodes protect the clock signal buffers (31, 33) from current backflow from the capacitor. *See, e.g.*, col. 4, lines 14-20 of Toyonaga *et al.*

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Howard L. Bernstein
Registration No. 25,665

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

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Date: December 1, 2005